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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/711,170 | 08/30/2004 | Brent A. Anderson | BUR920040040US1 | 5169 |

29154 7590 09/30/2005

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| EXAMINER |
|---|
| HO, HOANG QUAN TRAN |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2818 | |

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/711,170 | ANDERSON ET AL. | |
| | Examiner | Art Unit | |
| | Hoang-Quan Ho | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/02/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 – 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claim 1, the word "adjacent" does not have a clear meaning, whether it means near by without contact or two surfaces touching together. Regarding claims 2 – 9, they are dependent from claim 1. Hereinafter, the Office will take the world "adjacent" to be near by, not necessary touching.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 – 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Fried et al. (U.S. Pat. Pub. 2003/0178670).

Regarding claim 1, Fig. 11 of Fried teaches a field effect transistor (FET) comprising:

a fin structure (105; Para. 0026);

conducting spacers (115; Para. 0032; Para. 0045) positioned adjacent to said fin structure (105);

an insulator (110; Para. 0038) adjacent to said spacers (115); and

a gate layer (120; Para. 0038) positioned on said fin structure (105), said spacers (115), and said insulator (110).

Regarding claim 2, Fried teaches the FET, further comprising:

a substrate (90; Para. 0024); and

an isolation layer (99; Para. 0024) positioned over said substrate (90; Para. 0024),

wherein said isolation layer (99; Para. 0024) is positioned under said insulator (110), said spacers (115), and said fin structure (105) (Para. 0035; Fig. 10; Fig. 1, Steps 1 - 6).

Regarding claim 3, Fried teaches the FET, further comprising source/drain regions above said isolation layer (Para. 0041).

Regarding claim 4, Fried teaches wherein said fin structure (105) comprises an oxide layer (102; Para. 0026) over a silicon layer (100; Para. 0028).

Regarding claim 5, Fried teaches the FET, further comprising an oxide layer (116; Para. 0038) adjacent to said fin structure (105).

Regarding claim 6, Fried teaches the FET, further comprising a second oxide layer (101; Para. 0026) over said oxide layer (102; Para. 0026), wherein said second oxide layer is planar to said gate layer (Fig. 11). Fried teaches that the cap 101 is an insulator and any hard mask material can be applied to form cap 101 (Para. 0026). Fried also teaches that oxide shape 102 may have cap 101 (Para. 0026). Fig. 11 shows that oxide shape 102 is planar to gate layer, touching back to back.

Regarding claims 7 and 8, Fried teaches the FET, wherein said spacers (115; Para. 0032) and said gate layer (120; Para. 0034) comprise the same material. Fried discloses that the material is polysilicon.

Regarding claim 9, Fried teaches the FET, further comprising a gate insulator (116; Para. 0038) positioned between said fin structure (105) and said spacer (115).

Claims 1 – 5, 9 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (U.S. Pat. Pub. 2003/0042531).

Regarding claim 1, Fig. 5d of Lee teaches a field effect transistor (FET) comprising:

a fin structure (26; Para. 0086);

conducting spacers (38; Para. 0038) positioned adjacent to said fin structure (26);

an insulator (34; Para. 0084) adjacent to said spacers (38); and

a gate layer (36; Para. 0084) positioned on said fin structure (26), said spacers (38), and said insulator (34).

Regarding claim 2, Fig. 5d of Lee teaches the FET, further comprising:

a substrate (10; Para. 0067); and

an isolation layer (22; Para. 0067) positioned over said substrate (10),

wherein said isolation layer (22) is positioned under said insulator (34), said spacers (38), and said fin structure (26).

Regarding claim 3, Lee teaches the FET, further comprising source/drain regions (Para. 0058) above said isolation layer (22).

Regarding claim 4, Lee teaches the FET, wherein said fin structure comprises an oxide layer (30; Para 0058) over a silicon layer (26; Para. 0069).

Regarding claim 5, Fig. 5d of Lee teaches the FET, further comprising an oxide layer (30; Para. 0063) adjacent to said fin structure (26).

Regarding claim 9, Fig. 5d of Lee teaches the FET, further comprising a gate insulator (42; Para. 0077) positioned between said fin structure (26) and said spacers (38).

Regarding claim 10, Fig. 5d of Lee teaches the FET, further comprising a second insulator (30; Para. 0074) adjacent to said insulator (34).

Claims 11 – 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Mathew et al. (U.S. Pat. Pub. 2005/0098822).

Regarding claim 11, Fig. 4 of Mathew teaches a field effect transistor (FET) device comprising:

a fin structure (14; Para. 0018);

a first gate electrode (18; Para. 0018) adjacent to said fin structure (14);

a gate insulator (16; Para. 0018) positioned between said first gate electrode (18) and said fin structure (14);

a second gate electrode (44; Para. 0021) positioned transverse to said first gate electrode (18); and

a third gate electrode (42; Para. 0021) positioned on said fin structure (14), said first gate electrode (18), and said second gate electrode (44).

Regarding claim 12, Fig. 4 of Mathew teaches a FET, further comprising:

a substrate (15; Para. 0018); and

an isolation layer (13; Para. 0018) positioned over said substrate (15),

wherein said isolation layer (13) is positioned beneath said gate insulator (16), said first gate electrode (18), and said fin structure (14).

Regarding claim 13, Mathew teaches a FET, wherein said isolation layer is isolated from said second gate electrode (Para. 0022). Mathew discloses that sidewall spacers may be formed adjacent to the second gate, therefore a sidewall may be made be in between the second gate and the isolation layer.

Regarding claim 14, Fig. 5 of Mathew teaches a FET, further comprising source/drain regions (70 and 72; Para. 0022) above said isolation layer (13).

Regarding claim 15, Fig. 6 of Mathew teaches a FET, further comprising a dielectric material (66; Para. 0023) sandwiching said second gate electrode (44).

Regarding claim 16, Fig. 6 of Mathew teaches a FET, wherein said fin structure (14) comprises an oxide layer (16; Para. 0018) over a silicon layer (14; Para. 0018).

Regarding claim 17, Fig. 6 of Mathew teaches a FET, further comprising an oxide layer (26; Para. 0019) adjacent to said fin structure (14).

Regarding claim 18, Fig. 6 of Mathew teaches a FET, further comprising a second oxide layer (28; Para. 0019) over said oxide layer (26), wherein said second oxide layer (28) is planar to said third gate electrode (42).

Regarding claims 19 and 20, Mathew teaches a FET, wherein said first gate electrode and said third gate electrode comprise the same material (Para. 0022; Para. 0036). Mathew discloses that the material can be polysilicon.

Regarding claim 21, Fig. 4 of Mathew teaches a method of lowering a gate capacitance and extrinsic resistance in a field effect transistor (FET), said method comprising:

forming a fin structure (14; Para. 0018);

configuring a first gate electrode (18; Para. 0018) adjacent to said fin structure (14);

disposing a gate insulator (16; Para. 0018) between said first gate electrode (18) and said fin structure (14);

positioning a second gate electrode (44; Para. 0021) transverse to said first gate electrode (18); and

depositing a third gate electrode (42; Para. 0021) on said fin structure (14), said first gate electrode (18), and said second gate electrode (44).

Regarding claim 22, Fig. 4 of Mathew teaches a FET, further comprising forming an isolation layer (13; Para. 0018) over a substrate (15; Para. 0018), wherein said isolation layer (13) comprises a buried oxide (BOX) layer (Para. 0018), and wherein said isolation layer (13) is positioned beneath said gate insulator (16), said first gate electrode (18) and said fin structure (14).

Regarding claim 23, Fig. 5 Mathew teaches a FET, further comprising configuring source/drain regions (70 and 72; Para. 0022) above said isolation layer (13).

Regarding claim 24, Fig. 6 of Mathew teaches a FET, further comprising sandwiching said second gate electrode (44) with a dielectric material (66; Para. 0023).

Regarding claim 25, Fig. 6 of Mathew teaches a FET, wherein said fin structure (14) is formed by depositing an oxide layer (16; Para. 0018) over a silicon layer (14; Para. 0018).

Regarding claim 26, Fig. 6 of Mathew teaches a FET, further comprising forming an oxide layer (26; Para. 0019) adjacent to said fin structure (14).

Regarding claim 27, Fig. 6 of Mathew teaches a FET, further comprising forming a second oxide layer (28; Para. 0019) over said oxide layer (26), wherein said second oxide layer (28) is planar to said third gate electrode (42).

Regarding claims 28 and 29, Mathew teaches a FET, further comprising using the same material to form said first gate electrode and said third gate electrode (Para. 0022; Para. 0036). Mathew discloses that the material can be polysilicon.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoang-Quan Ho whose telephone number is (571) 272-0237. The examiner can normally be reached on Monday - Friday, 8AM - 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HQH
September 15, 2005

GEORGE ECKERT
PRIMARY EXAMINER